REMARKS

This application contains claims 1-51. Claims 1-3,

6, 8, 11, 14-16, 18-20, 23, 25, 28, 31-33, 35-37, 40, 42, 45

and 48-50 are hereby amended. No new matter has been added.

Reconsideration is respectfully requested.

Applicant thanks Examiners Guill and Rodriguez for

the courtesy of a personal interview with Applicant's

representative, Sanford T. Colb (Reg. No. 26,856), held in the

USPTO on December 14, 2005. At the interview, Mr. Colb

pointed out the Written Description of the claimed invention

as it appears in the specification as filed. Mr. Colb also

explained that the software debugging techniques of Bruegge

and Ball (cited below) could not have been combined with the

hardware-oriented formal verification techniques described by

Beer (also cited below). It was agreed that Applicant would

amend claim 1 to read, "providing a specification of a path to

be found," rather than "specifying a path to be traversed,"

and that references to a "system under study" in the claims

would be amended to refer to a "hardware system under study."

The Examiners agreed that these amendments would overcome the

present rejections under 35 U.S.C. 103(a) and 35 U.S.C. 112.

The specification was objected to for certain

informalities on pages 9 and 16. Applicant has amended the

specification in order to overcome this objection. The

amendment to the specification on page 9 mirrors a similar

amendment made to claims 11, 28 and 45, which is explained

below.

Claims 3, 6, 8, 14, 20, 23, 25, 31, 37, 40, 42 and

48 were objected to for informalities. Applicant has amended

these claims as suggested by the Examiner in order to overcome

these objections.

Claims 1, 13, 18, 30, 35 and 47 were rejected under

35 U.S.C. 112, first paragraph, for failing to comply with the

Written Description requirement. Applicant has amended

independent claims 1, 18 and 35, as agreed in the interview,

in order to clarify that the invention is based on a

specification of a path to be found through the states of the

system. Applicant respectfully traverses the rejection of

dependent claims 13, 30 and 47.

With regard to claims 1, 18 and 35, the Examiner

alleged that the specification fails to disclose that a

specified sequence of events must occur on a specified path,

and that the specification appears to disclose only computing

successive reachable steps with no constraint that events

occur in the specified sequence. In response to this

rejection, Applicant points out that the Summary of the

Invention states explicitly that "The model checker uses

techniques of on-the-fly model checking to find a path through

the reachable state space on which all the events occur in the order given by the specification, as it proceeds to explore the state space of the system" (page 7, lines 9-13). Fig. 3 shows such a path 58 through successive sets of states S_0, S_1, ..., S_9 in a state space 48, on which events 60, 62 and 64 occur in the sequence that is specified in Fig. 2. Applicant has amended claims 1, 18 and 35 to use the literal language of the description in the Summary of the Invention. In view of this amendment, Applicant believes that the rejection of claims 1, 18 and 35 should be withdrawn.

With regard to claims 13, 30 and 47, the Examiner alleged again that the specification fails to disclose that a specified sequence of events must occur on a specified path. As explained above, these aspects of the present invention are disclosed in the Summary of the Invention and in Figs. 2 and 3. Therefore, Applicant believes that the rejection of claims 13, 30 and 47 should be withdrawn, as well.

Claims 11, 28 and 45 were rejected under 35 U.S.C. 112, second paragraph, for being indefinite. Applicant has amended these claims by changing the order of phrases in the claims in order to clarify the claim language and thus to overcome this rejection. The amended claim language states that in producing the partial trace, the predecessor state to the state in the first set is chosen in the initial set. This

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amendment is supported by the example shown in Fig. 3 and is

the opposite of the interpretation proposed by the Examiner

(that the predecessor state in the initial set is chosen to be

the state in the first set). In view of this amendment,

claims 11, 28 and 45 are now believed to meet the requirements

of 35 U.S.C. 112.

Claims 1-3, 6-20, 23-37 and 40-51 were rejected

under 35 U.S.C. 103(a) over Beer et al. ("RuleBase: An

Industry-Oriented Formal Verification Tool") in view of

Bruegge et al. ("Generalized Path Expressions: A High Level

Debugging Mechanism") and further in view of Ball et al.

("Optimally Profiling and Tracing Programs"). Applicant has

amended independent claims 1, 18 and 35, as agreed in the

interview, in order to clarify the distinction of the claimed

invention over the cited art. The dependent claims have also

been amended as necessary to accord with the amended language

of the independent claims.

Claim 1, as amended, recites a method for checking a

model, which defines states of a hardware system under study

and a transition relation among the states. (The specific

recitation of a hardware system is supported literally in the

specification on page 13, lines 12-16.) A path to be

traversed through the states is specified, from an initial set

of the states to a target set, such that a specified sequence

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of events is to occur on this path. Successive reachable sets

of the states of the system are computed along the specified

path. If no intersection is found to exist between the

reachable sets on the specified path and the target set, a

partial trace along the specified path is produced between at

least one initial state and a termination state in which at

least one of the specified events occurs.

Beer describes a tool for formal verification of

hardware design (section 1, Introduction, first and second

paragraphs). The tool was developed for use in conjunction

with hardware design methodologies (section 2.1, Design for

Formal Verification). RuleBase supports hardware description

languages (section 3, The RuleBase Tool, third paragraph).

RuleBase is used both in unit-level verification of hardware

designs and in verification of system-level hardware

architecture (section 1, sixth paragraph, as well as section

5.2). It should be noted that because formal verification

deals with finite-state systems having deterministic

transition relations, it is well suited for hardware

verification, but was not generally considered suitable for

software verification at the time of filing of the present

patent application. Beer makes no suggestion that his tool

could be used in software design.

Bruegge describes a mechanism for debugging software programs using generalized path expressions (section 1, Introduction, second and third paragraphs). This mechanism uses path rules to monitor the behavior of a computation and to trigger actions to be performed (section 3, Path Rules, first paragraph). Path rules may be used either to find or to enforce a particular execution sequence (section 3.1, Generalized Path Expressions, second and third paragraphs). These rules are clearly directed to analyzing and controlling the progress of a software process. Bruegge neither teaches nor suggests that his debugging mechanism could be used in hardware verification.

Ball describes algorithms for inserting monitoring code to profile and trace programs (abstract). These algorithms require that a program be instrumented (by addition of tracing code to the program) in order to record the sequence of executed basic blocks as the program runs. In other words, each basic block is instrumented so that whenever it executes, it writes a "witness" to a trace file (page 1338, section 4, Program Tracing, first paragraph). Thus, Ball's techniques are clearly and explicitly limited to the field of software program debugging. There is no way that a hardware design could be "instrumented" to write a trace file as Ball describes.

Thus, whereas Beer describes a particular method for
<u>formal verification of a hardware design</u>, Bruegge and Ball are
directed specifically and exclusively to methods for <u>debugging</u>
<u>software</u>. A person of ordinary skill in the art in either of
these fields would not have been motivated to combine these
disparate techniques and, even had the person been so
motivated, could not possibly have done so. Interpolating
Ball's technique into Beer, for example, would have required
that a hardware design under test be somehow annotated with
software commands so that the hardware design generates a
software trace file. As noted in MPEP 2143.02:

> THE PROPOSED MODIFICATION CANNOT CHANGE THE
> PRINCIPLE OF OPERATION OF A REFERENCE
>
> If the proposed modification or combination of the
> prior art would change the principle of operation of
> the prior art invention being modified, then the
> teachings of the references are not sufficient to
> render the claims *prima facie* obvious. *In re Ratti*,
> 270 F.2d 810, 123 USPQ 349 (CCPA 1959).

Even if it were possible to use Bruegge and Ball's software
debugging techniques in Beer's system, such a modification
would change completely Beer's principles of operation.
Therefore, the cited references cannot be combined to arrive
at the method of claim 1, and claim 1 is thus patentable over
the art of record.

Independent claims 18 and 35 recite apparatus and a
computer software product, which operate on principles similar

to the method of claim 1. These independent apparatus and

software claims are believed to be patentable, as well, for

the reasons explained above.

Claims 2, 3, 6-17, 19, 20, 23-34, 36, 37 and 40-51

depend directly or indirectly from independent claims 1, 18

and 35. In view of the patentability of the independent

claims, as explained above, these dependent claims are also

believed to be patentable.

Claims 4, 5, 21, 22, 38 and 39 were rejected under

35 U.S.C. 103(a) over Beer in view of Bruegge and Ball and

further in view of Beer et al. ("On-the-fly Model Checking of

RCTL Formulas"). In view of the patentability of independent

claims 1, 18 and 35, dependent claims 4, 5, 21, 22, 38 and 39

are likewise believed to be patentable.

Furthermore, the dependent claims in this

application are believed to recite subject matter that is

independently patentable, notwithstanding the patentability of

the independent claims. In the interest of brevity, however,

Applicant will not argue the specific patentability of the

dependent claims at this point.

Applicant has studied the additional reference made

of record by the Examiner and considers the claims in this

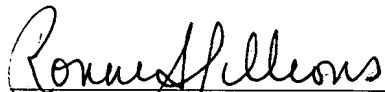application to be patentable over this reference, as well,

whether the reference is taken individually or in combination with the other cited references.

Applicant believes the amendments and remarks presented hereinabove to be fully responsive to all of the objections and grounds of rejection raised by the Examiner. In view of these amendments and remarks, Applicant respectfully submits that all of the claims in the present application are in order for allowance. Notice to this effect is hereby requested.

If the Examiner has any questions he is invited to contact the undersigned at 202-628-5197.

Respectfully submitted,

BROWDY AND NEIMARK, P.L.L.C.
Attorneys for Applicant

By _Ronni S. Jillions_

Ronni S. Jillions
Registration No. 31,979

RSJ:rsj
Telephone No.: (202) 628-5197
Facsimile No.: (202) 737-3528
G:\BN\C\colb\Ben-David1\PTO\2005Dec21 AMD.doc